High Performance Embedded Architectures and Compilers: 5th International Conference, HiPEAC 2010, Pisa, Italy, January 25-27, 2010, Proceedings (Lecture Notes in Computer Science)

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This book constitutes the refereed proceedings of the 5th International Conference on High Performance Embedded Architectures and Compilers, HiPEAC 2010, held in Pisa, Italy, in January 2010. The 23 revised full papers presented together with the abstracts of 2 invited keynote addresses were carefully reviewed and selected from 94 submissions. The papers are organized in topical sections on architectural support for concurrency; compilation and runtime systems; reconfigurable and customized architectures; multicore efficiency, reliability, and power; memory organization and optimization; and programming and analysis of accelerators.

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